## DISPLAY CONTROLLER CARD

# BT-074

# *Users Manual*

Version : 03

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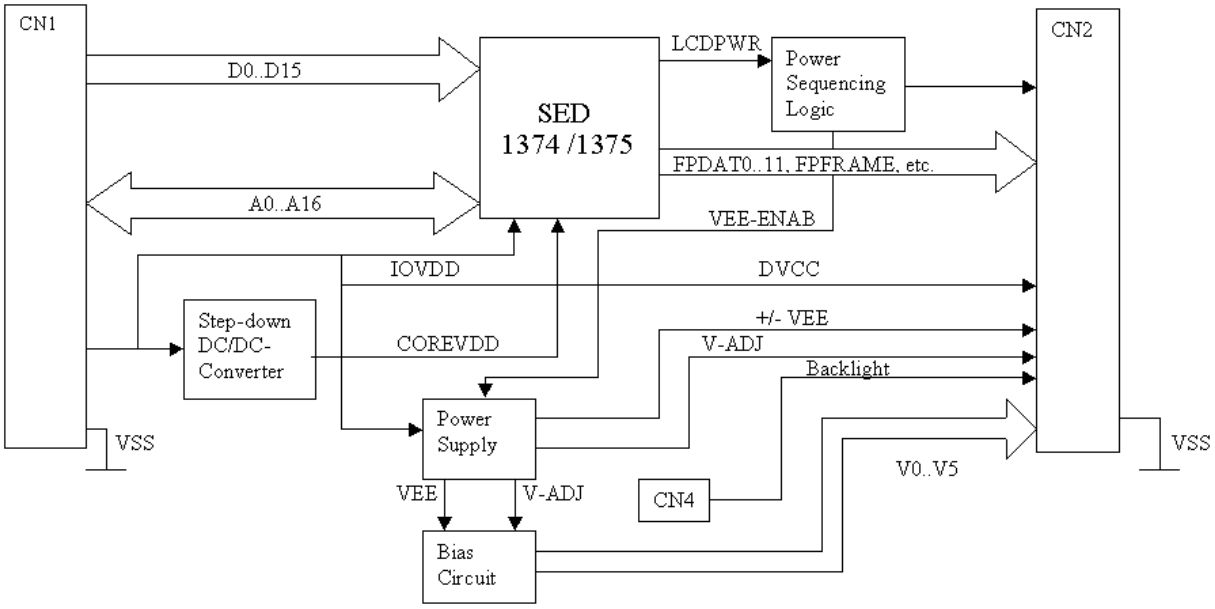
# 1 GENERAL DESCRIPTION

The BT-074 is a LCD-Controller-Board for many types of controller-less displays (monochrome, passive colour, TFT). It has an 16 bit µC-Interface (optional 8 bit) supporting the following busses: SH3/SH4, MC68K, Generic #1/ Generic #2. It also features a temperature compensated contrast adjustment voltage generation, as well as an additional bias voltage circuit. There are two types of controllers which can be used on this board: either a SED 1374 or SED 1375 (SED 1374 with 40K, SED 1375 with 80K display buffer on chip). The features of the BT-074 are:

- up to 256 simultaneous colors from a possible 4096 colors on passive LCD panels and TFT Displays
- up to 16 grey shades on monochrome Displays
- supports 3,3V or 5V displays
- supports 3,3V or 5V µC-Interfaces (for using a 3,3V µC-Interface an additional 5V power supply is necessary)
- Resolutions from 320x 240 at a color depth of 8 bpp to 640x480 at a color depth of 2 bpp
- Hardware Portrait Mode
- Split Screen Display
- Virtual Display Support (panning and scrolling)
- LCD power-down sequencing
- Register level support for EL panels
- Positive (up to ca. 33V) or negative (up to ca. –28,5 V) LCD power supply can be selected with jumpers.

For a detailled description of some of the features mentioned above please refer to the SED 1374 or SED 1375 manual.

## 2 BLOCK DIAGRAM



# 3 SIGNAL DESCRIPTION

## 3.1 Electrical Characteristics

| ITEM | SYMBOL | RATING |
|---|---|---|
| Supply Voltage | VCC | 3,3V / 5V (**note1**) |
| Input Voltage | Vin | 3,3V / 5V (**note2**) |
| Bus Clock Frequency | BCLK | T.B.D. |
| Current Consumption (VCC = 5V) | I | 200mA |
| Power Dissipation (VCC = 5V) | Pdisp | 1W |

**Note 1:** If this controller card is used with a 3,3V µController Interface an additional power supply of 5V is required.
**Note 2:** The Input Voltage Range is strongly dependent on the actual display. The absolute maximum rating for the
BT-074 without a display connected is 0..7V.

## 3.2 Connector Overview

| Symbol | Description |
|---|---|
| CN1 | µC-Interface |
| CN2 | LCD-Interface |
| CN3 | Signal Matrix |
| CN4 | Inverter-Interface |

## 3.3 Connector CN1 (Connection to µC-Interface)

| PIN | NAME | SIGNAL DESCRIPTION |
|---|---|---|
| 0-15 | D[0:15] | Data Input (these pins are directly connected with DB[0:15] of SED1374/5) |
| 16-32 | A[0:15] | Address bits (these pins are directly connected to AB[15:0] of SED1374/5.) |
| 33 | A16 | A16 for SED1375, for SED1374 see LP1 |
| 34 | /BS | see Jumper Settings LP11, LP12 |
| 35 | /RES | This pin inputs the Reset Signal |
| 36 | /CS | This pin inputs the Chip Select (decoding logic necessary if used with MC68K or Generic#2 interface; refer to SED1374/5 manual) |
| 37 | /RD | /RD (LP7); RD/WR (LP8,LP10) |
| 38 | /WE1 | This pin inputs the write enable signal for upper data byte |
| 39 | /WE0 | This pin inputs the write enable signal for lower data byte (see LP9) |
| 40 | /WAIT | wait signal |
| 41 | RD/WR | RD/WR (see LP8,LP10) |
| 42 | VCC | 3,3V / 5V supply voltage |
| 43 | GND | GND |
| 44 | BCLK | BUS-Clock |

## 3.4 Connector CN2 (Connection to LCD Module)

| PIN | SYMBOL | SIGNAL DESCRIPTION |
|---|---|---|
| 1 | GND | VSS |
| 2 | n.c . | left open |
| 3 | GPIO | General Purpose I/O Pin #0 |
| 4 | DD11 | Display Data Pin/ General Purpose I/O Pin #4 |
| 5 | DD10 | Display Data Pin/ General Purpose I/O Pin #3 |
| 6 | DD9 | Display Data Pin/ General Purpose I/O Pin #2 |
| 7 | DD8 | Display Data Pin/ General Purpose I/O Pin #1 |
| 8 | GND | VSS |
| 9 | DD3 | Display Data Pin |
| 10 | DD2 | Display Data Pin |
| 11 | DD1 | Display Data Pin |
| 12 | DD0 | Display Data Pin |
| 13 | DD7 | Display Data Pin |
| 14 | DD6 | Display Data Pin |
| 15 | DD5 | Display Data Pin |
| 16 | DD4 | Display Data Pin |
| 17 | GND | VSS |
| 18 | /CLP | Shift Clock (neg.) |
| 19 | CLP | Shift Clock |
| 20 | FRP | Frame Pulse |
| 21 | M | Multiple Functions:<br>- TFTs: Display Enable (DRDY)<br>- LCD Backplane Bias (MOD)<br>- Second Shift Clock (FPSHIFT2) |
| 22 | LIP | Line Pulse |
| 23 | DEN | Display Enable |
| 24 | GND | VSS |
| 25 | DVCC | Display Logic Power Supply |
| 26 | VEE | Display Driving Voltage (see LP13) |
| 27 | V-ADJ | Contrast Adjustment Voltage |
| 28 | GND | VSS |
| 29 | VEE | Display Driving Voltage (see LP13) |
| 30 | +12V | Inverter Power Supply |
| 31 | /DEN | Display Enable (neg.) |
| 32 | V0 | Bias Voltage |
| 33 | V2 | Bias Voltage |
| 34 | V1 | Bias Voltage |
| 35 | V4 | Bias Voltage |
| 36 | V3 | Bias Voltage |
| 37 | V5 | Bias Voltage |
| 38 | GND | VSS |

## 3.5 Connector CN 3 (Signal Matrix)

This Connector can be used to change the Pin Mapping of Connector CN2 in order to use other connection solutions.

## 3.6 Connector CN 4 (Inverter)

| PIN | SYMBOL | SIGNAL DESCRIPTION |
|---|---|---|
| 1 | +12V | Backlight driving voltage |
| 2 | n.c . | left open |
| 3 | GND | VSS |

## 3.7 LCD Interface Pin Mapping

| | Monochrome Passive Panel | | | Color Passive Panel | | | | Color TFT/MD-TFT | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SED 1375 Pin Name | 4-bit Single | 8-bit Single | 8- bit Dual | 4-bit Single | 8-bit Single Format 1 | 8-bit Single Format 2 | 8-bit Dual | 9-bit | 12-bit | 15-bit | 18-bit |
| FPFRAME | FPFRAME | | | | | | | | | | |
| FPLINE | FPLINE | | | | | | | | | | |
| FPSHIFT | FPSHIFT | | | | | | | | | | |
| DRDY | MOD | MOD | MOD | MOD | FPSHIFT2 | MOD | MOD | DRDY | | | |
| FPDAT0 | driven 0 | D0 | LD0 | driven 0 | D0 | D0 | LD0 | R2 | R3 | R4 | R5 |
| FPDAT1 | driven 0 | D1 | LD1 | driven 0 | D1 | D1 | LD1 | R1 | R2 | R3 | R4 |
| FPDAT2 | driven 0 | D2 | LD2 | driven 0 | D2 | D2 | LD2 | R0 | R1 | R2 | R3 |
| FPDAT3 | driven 0 | D3 | LD3 | driven 0 | D3 | D3 | LD3 | G2 | G3 | G4 | G5 |
| FPDAT4 | D0 | D4 | UD0 | D0 | D4 | D4 | UD0 | G1 | G2 | G3 | G4 |
| FPDAT5 | D1 | D5 | UD1 | D1 | D5 | D5 | UD1 | G0 | G1 | G2 | G3 |
| FPDAT6 | D2 | D6 | UD2 | D2 | D6 | D6 | UD2 | B2 | B3 | B4 | B5 |
| FPDAT7 | D3 | D7 | UD3 | D3 | D7 | D7 | UD3 | B1 | B2 | B3 | B4 |
| FPDAT8 | GPIO1 | GPIO1 | GPIO1 | GPIO1 | GPIO1 | GPIO1 | GPIO1 | B0 | B1 | B2 | B3 |
| FPDAT9 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | GPIO2 | R0 | R1 | R2 |
| FPDAT10 | GPIO3 | GPIO3 | GPIO3 | GPIO3 | GPIO3 | GPIO3 | GPIO3 | GPIO3 | G0 | G1 | G2 |
| FPDAT11 | GPIO4/ Hardware Video Invert | GPIO4/ Hardware Video Invert | GPIO4/ Hardware Video Invert | GPIO4/ Hardware Video Invert | GPIO4/ Hardware Video Invert | GPIO4/ Hardware Video Invert | GPIO4/ Hardware Video Invert | GPIO4 | B0 | B1 | B2 |

# 4 FUNCTION OF POTENTIOMETERS

Potentiometer P1: This potentiometer is used for adjusting the driving voltage of LCD's.

Potentiometer P2: This potentiometer is used for adjusting the positive contrast voltage. This voltage is less or equal than VEE.

Potentiometer P3: This potentiometer is used for adjusting the negative contrast voltage. The amount of this voltage can not be higher than VEE.

Potentiometer P4: This potentiometer is used for adjusting the temperature compensation of the contrast voltage to the actual display.

# 5 PRE TURN ON CHECKLIST

Before connecting the BT-047 LCD-Controllerboard, please read the following informations carefully:

- Check Jumper settings (refer to the following section).
- Check connection of Pin 1 of connector CN 1.
- Check supply voltages:
  ~ Adjust VEE with P1 so that it is ca. 2 Volts above the recommended LCD-supply voltage, but well below the highest possible input voltage of the display.
  ~ Turn P4 to adjust the gradient of the temperature compensation.
  ~ Adjust V-ADJ with P2 (in case of a positive supply voltage) or with P3 (in case of a negative supply voltage) to receive the optimal contrast.
- Check connection of Pin 1 of connector CN 2.

# 6 JUMPER SETTINGS

## 6.1 Jumper Setting for Controller Selection

| LP1 | Controller (AB16) |
|---|---|
| 1/2 | IOVDD (SED 1374) |
| 2/3 | A16 CN1 (SED 1375) |

## 6.2 Input & Output-Voltage

| LP22 | µController-Interface (IOVDD) |
|---|---|
| 1/2 | 5V (Vcc) |
| 2/3 | 3,3V |

| LP2 | LCD-Interface (DVCC) |
|---|---|
| 1/2 | 5V |
| 2/3 | 3,3V |

## 6.3 µC Interface

| LP3 | µController |
|---|---|
| 2/3 | Little Endian |
| 1/2 | Big Endian **(default)** |

**note:** BT-2000 is “Big Endian”.

| LP7 | /RD (PIN76 SED137x) |
|---|---|
| ½ | IOVDD |
| 2/3 | /RD (CN1.37) |

| LP8 | LP10 | RD/WR (PIN79 SED137x) |
|---|---|---|
| ½ | 1/2 | IOVDD |
| ½ | 2/3 | CN1.41 |
| 2/3 | 1/2 | IOVDD |
| 2/3 | 2/3 | CN1.37 |

| LP9 | /WE0 (PIN77 SED137x) |
|---|---|
| ½ | IOVDD |
| 2/3 | /RD (CN1.37) |

| LP11 | LP12 | /BS (PIN75 SED137x) |
|---|---|---|
| ½ | 1/2 | IOVDD |
| ½ | 2/3 | GND |
| 2/3 | 1/2 | CN1.34 |
| 2/3 | 2/3 | GND |

## 6.4 Jumper Settings for Host-Bus Selection

| LP4 | LP5 | LP6 | LP7 | LP8 | LP9 | LP10 | LP11 | LP12 | Host Bus |
|---|---|---|---|---|---|---|---|---|---|
| 2/3 | 2/3 | 2/3 | 2/3 | 1/2 | 2/3 | 2/3 | 2/3 | 1/2 | SH-4 interface |
| 2/3 | 2/3 | 1/2 | 2/3 | 1/2 | 2/3 | 2/3 | 2/3 | 1/2 | SH-3 interface |
| 2/3 | 1/2 | 2/3 | x | x | x | x | x | x | reserved |
| 2/3 | 1/2 | 1/2 | 1/2 | 1/2 | 1/2 | 2/3 | 2/3 | 1/2 | MC68K #1, 16-bit |
| 1/2 | 2/3 | 2/3 | x | x | x | x | x | x | reserved |
| 1/2 | 2/3 | 1/2 | 2/3 | 1/2 | 2/3 | 2/3 | 2/3 | 1/2 | MC68K #2, 16-bit |
| 1/2 | 1/2 | 2/3 | x | x | x | x | x | x | reserved |
| 1/2 | 1/2 | 2/3 | x | x | x | x | x | x | reserved |
| 1/2 | 1/2 | 1/2 | 2/3 | 2/3 | 2/3 | 2/3 | 2/3 | 2/3 | Generic #1, 16-bit |
| 1/2 | 1/2 | 1/2 | 2/3 | 1/2 | 2/3 | 1/2 | 1/2 | 1/2 | Generic #2, 16-bit |
| 1/2 | 1/2 | 1/2 | 2/3 | 2/3 | 2/3 | 2/3 | 2/3 | 2/3 | BT-2000 **(default)** |

## 6.5 Jumper Setting For Display Selection

$V_{EE}$ /$V_{Adj}$ ($V_0$) at CN2.26/29

| LP13 | CN2.26/29 |
|---|---|
| 1/2 | $V_{EE}$ |
| 2/3 | $V_{Adj}$ ($V_0$) |

LCD-Power supply

| LP14 | LP15 | LP16 | LP17 | LP18 | LP19 | Polarity of VEE |
|---|---|---|---|---|---|---|
| 1/2 | 1/2 | 1/2 | 1/2 | 1/2 | 2/3 | positive |
| 2/3 | 2/3 | 2/3 | 2/3 | 2/3 | 1/2 | negative |

Additional Bias Voltage Circuit

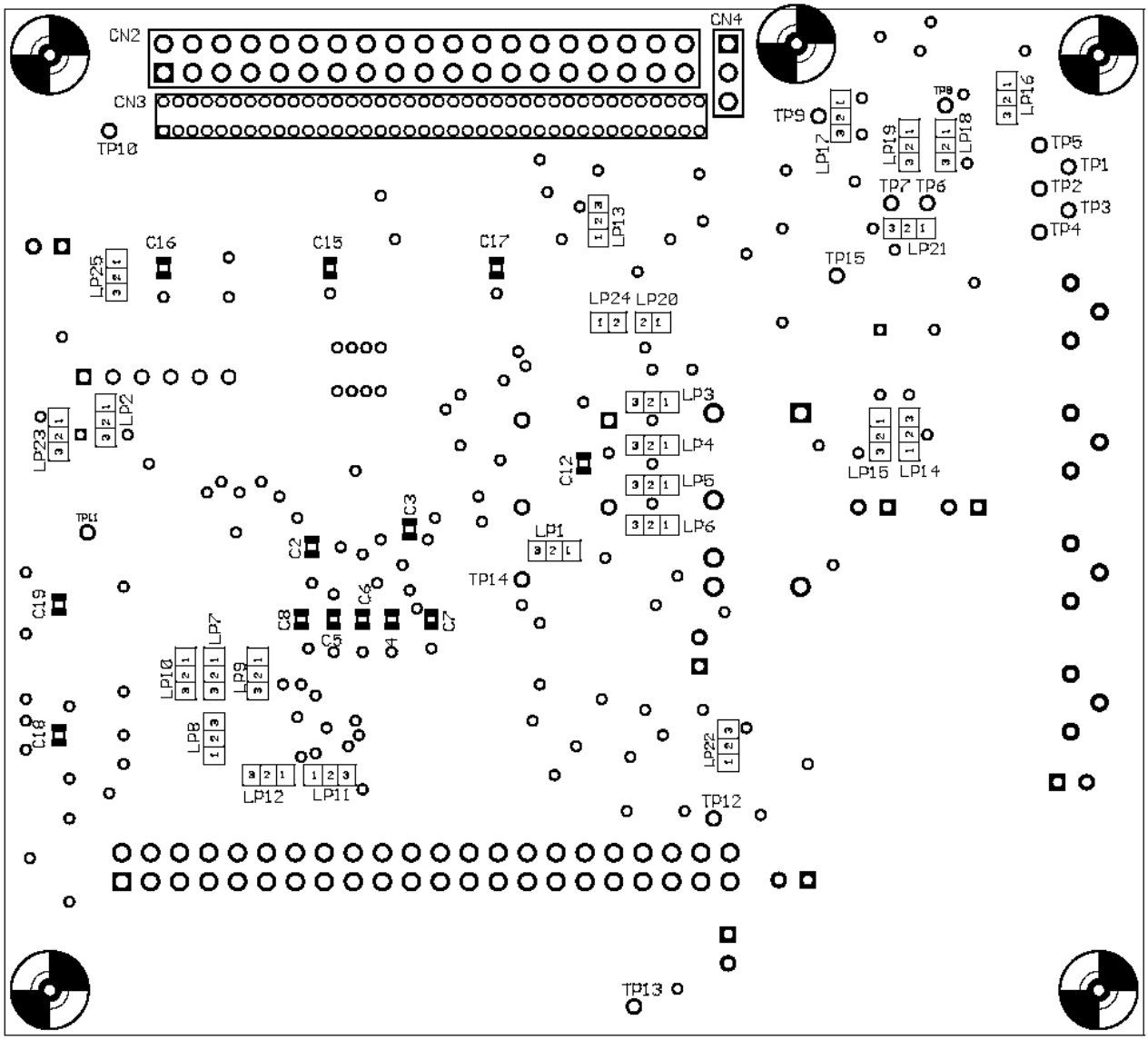
| LP20,LP24 | Bias Circuit |
|---|---|
| open | No |
| closed | Yes |

Temp.-Compensation with NTC/DS1847

| LP21 | Temp.-Compensation |
|---|---|
| 1/2 | NTC |
| 2/3 | DS1847 |

Voltage for line driver (DD8 – DD11; GPIO0)

| LP23 | LP25 | Function |
|---|---|---|
| 1/2 | 1/2 | output DVcc |
| 1/2 | 2/3 | Input DVcc **not allowed!!** |
| 2/3 | 1/2 | output I/$OV_{DD}$ |
| 2/3 | 2/3 | input I/$OV_{DD}$ |




Backside of the BT-074 with Jumpers

# 7 ADJUSTING THE BIAS CIRCUIT

In the default case the BT-074 is delivered with a bias circuit that is directly only suitable for the Kyocera KCS038 display, but small changes in hardware allow also the use of KRS025 and KCS043. In order to use a KRS025 the resistor R13 (with a value of 220 kΩ) has to be replaced by a 180kΩ (+/- 1.0 %) resistor. Using a KCS043 the resistors R11, R12, R14 and R15 have to be replaced by 8.1 kΩ (+/- 1.0 %) resistors and the resistor R13 has to be replaced by a 67.5 kΩ (+/- 5 %) resistor.

# 8 ADJUSTING THE TEMPERATURE COMPENSATION

Most passive LCD displays need a temperature compensated driving voltage to generate a proper contrast over the defined temperature range. The temperature compensation has to be adjusted to the temperature dependency of the specific display.This can either be done by adjusting the potentiometer P4 to achieve a linearized curve of the NTC-resistor R5 or replacing this resistor by one whose temperature gradient is more similar to that of the display. With the Dallas DS1847 it is possible to use a temperature gradient specified for.

# 9 INITIALIZATION

In order to generate proper display signals the BT-074 must be initialized, i.e. the control registers of the SED1374 or SED1375 controller must be set to a known state. For a detailled description of this process please refer to the SED1375 manual (Programming Notes and Examples, pg. 8). There are also several development tools to download free on Epsons homepage, especially a small program called cfg1375 to calculate the register values (http://www.erd.epson.com/vdc/RelSoft/1375/default.htm). We have already tested several displays with the Bt-074 (see listing below) and are therefore able to supply with the appropriate register values for those displays. Note that in order to achieve the recommended frame rate it can be necessary to change the input clock frequency by replacing the Oscillator X1 with a pin compatible one (The default version of the BT-074 comes with a 12MHz oscillator).

## 9.1 Input clock frequency CLKI

The following table shows the relation between frame rate and input clock frequency for several displays:

| Display | Resolution | Frame Rate | CLKI and FrameRate |
|---|---|---|---|
| KCS038 | 240x320 | 70-80Hz | 13 MHz (74Hz) or 6MHz (69 Hz) or 6,5 MHz (74Hz) |
| KCS043 | 320x120 | 70-80Hz | 6 MHz (71 Hz) |
| KCS057 | 320x240 | 70-80Hz | 12 MHz (71Hz) or 6MHz (71Hz) |
| KCS065 | 640x240 | 70-80Hz | 12MHz (74 Hz) or 24 MHz (74 Hz) |
| KRS025 | 160x240 | 70-80Hz | 3,456 MHz (75 Hz) or 12 MHz (75Hz), but HDNP = 0x0E and VNDP = 0x17 |
| LQ038 | 320x240 | ca. 70 Hz | 6 MHz (71 Hz) or 12 MHz (71 Hz) |
| LQ057 | 320x240 | ca. 70 Hz | 6 MHz (ca. 65Hz) or 12 MHz (71 Hz) |
| LM4Q30TA | 320x240 | 50-52Hz | 12MHz (52 Hz) HDNP = 10; VNDP = 27; or 4,309MHz (51 Hz) |
| LM5H40TD | 480x320 | 50-52Hz | 8,456 MHz (51 Hz) |
| SP14Q002-A1 | 320x240 | 70-80Hz | 6 MHz (71 Hz) oder 12 MHz (71 Hz) |
| SX19V001 | 640x480 | 80-120Hz | 40 MHz (124 Hz) oder 30 MHz (93Hz) |
| SX21V001 | 640x480 | 100-150Hz | 40 MHz (124 Hz) |
| LMG5278 | 640x480 | 120-140Hz | 40 MHz (124 Hz) |

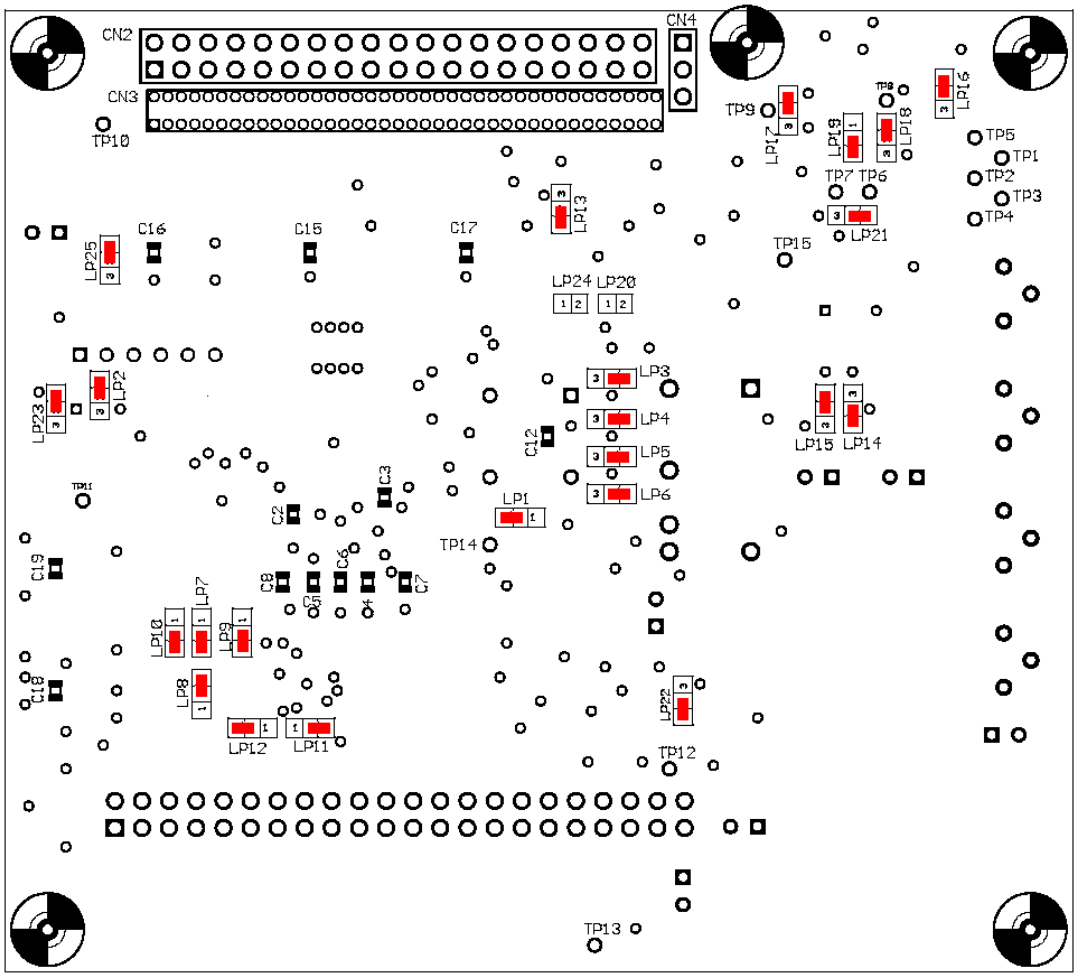
| | | | |
|---|---|---|---|
| LMG7550 | 640x480 | 69-110Hz (140Hz) | 40 MHz (124 Hz) or 30 MHz (93Hz) |
| LMG7525 | 320x240 | 70-140Hz | 12 MHz (71Hz) or 24 MHz (140 Hz) |
| PG320240C | 320x240 | 70-80Hz | 12 MHz (71 Hz) |
| MGS320240 | 320x240 | 70-80Hz | 12 MHz (71 Hz) |

## 9.2 Display Overview

At the moment the register values for the following displays are available:

- KCS 057
- LQ 057
- MGLS320240
- SP14

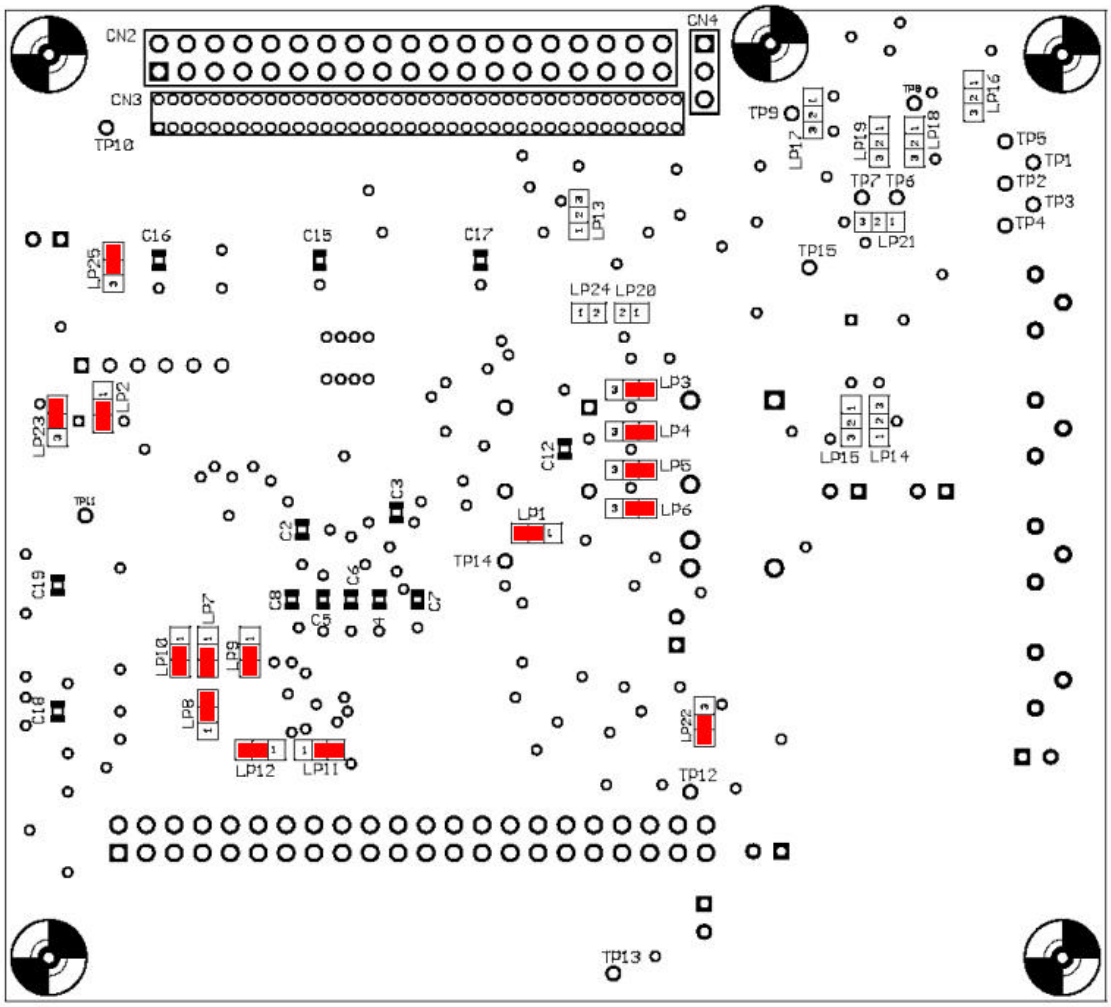
## 9.3 CSTN QVGA, 256 Colors, 5V, pos.$V_{EE}$ (KCS 057, LM057 a.e.)




| Register | Value | Register | Value |
|---|---|---|---|
| [01] Mode Register 0 | 0x3B | [0D] Screen 1 Start Adress (MSB) | 0x00 |
| [02] Mode Register 1 | 0xD0 | [0E] Screen 2 Start Adress (LSB) | 0x00 |
| [03] Mode Register 2 | 0x03 | [0CF] Screen 2 Start Adress (MSB) | 0x00 |
| [04] Horizontal Panel Size | 0x27 | [10] Start Adress (MSBs) | 0x00 |
| [05] Vertical Panel Size (LSB) | 0xEF | [11] Memory Adress Offset | 0x00 |
| [06] Vertical Panel Size (MSB) | 0x00 | [12] Screen 1 Vertical Size (LSB) | 0xFF |
| [07] FPLINE Start Position | 0x00 | [13] Screen 1 Vertical Size (MSB) | 0x03 |
| [08] Horizontal Non-Display Period | 0x00 | [18] GPIO Configuration Control | 0x00 |
| [09] FPFRAME Start Position | 0x00 | [19] GPIO Status/Control | 0x00 |
| [0A] Vertical Non-Display Period | 0x00 | [1A] Scratch Pad | 0x00 |
| [0B] MOD Rate | 0x00 | [1B] Portrait Mode | 0x00 |
| [0C] Screen 1 Start Adress (LSB) | 0x00 | [1C] Line Byte Count | 0x00 |

**Note:** These values result from a Frame Rate of 71 Hz, an input clock of 12 MHz and a 8 bit-per-pixel display mode.

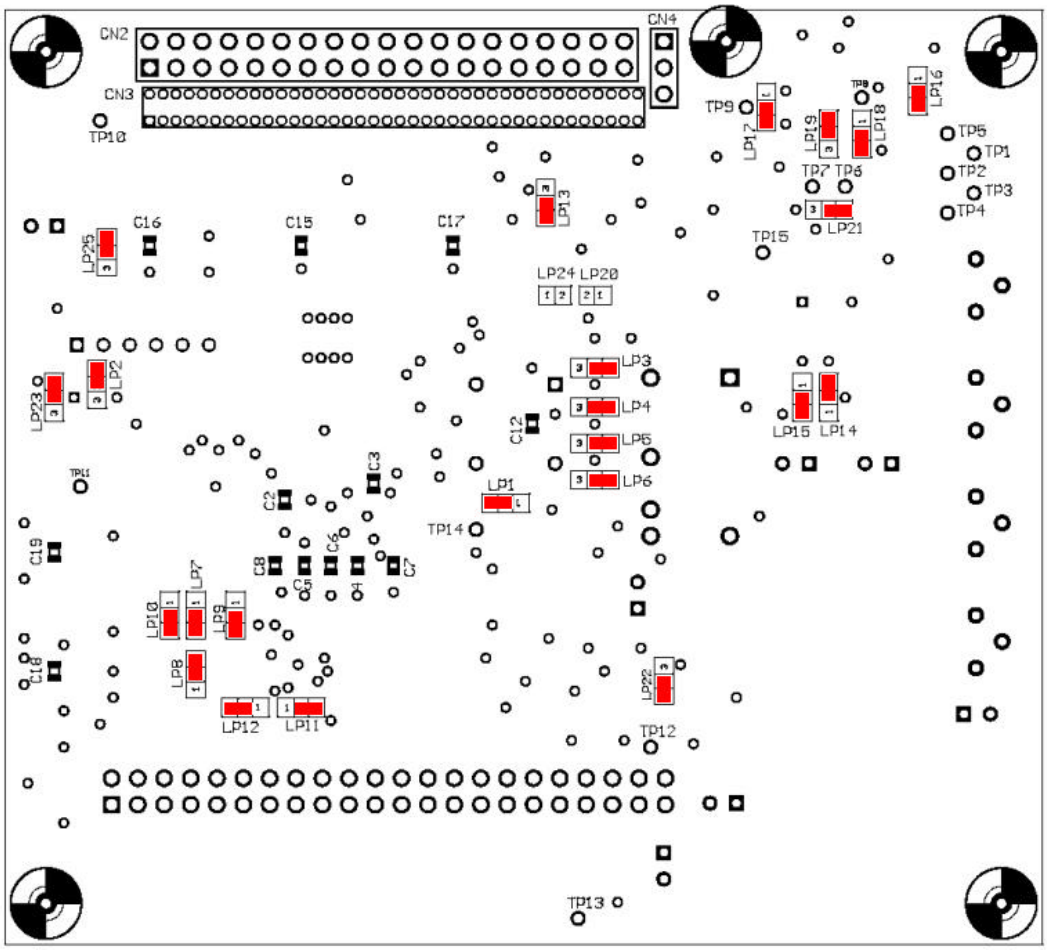
## 9.4 TFT QVGA, 256 Colors, 3,3V (LQ 057, a.e.)




| Register | Value | Register | Value |
|---|---|---|---|
| [01] Mode Register 0 | 0xA1 | [0D] Screen 1 Start Adress (MSB) | 0x00 |
| [02] Mode Register 1 | 0xD0 | [0E] Screen 2 Start Adress (LSB) | 0x00 |
| [03] Mode Register 2 | 0x03 | [0CF] Screen 2 Start Adress (MSB) | 0x00 |
| [04] Horizontal Panel Size | 0x27 | [10] Start Adress (MSBs) | 0x00 |
| [05] Vertical Panel Size (LSB) | 0xEF | [11] Memory Adress Offset | 0x00 |
| [06] Vertical Panel Size (MSB) | 0x00 | [12] Screen 1 Vertical Size (LSB) | 0xFF |
| [07] FPLINE Start Position | 0x00 | [13] Screen 1 Vertical Size (MSB) | 0x03 |
| [08] Horizontal Non-Display Period | 0x02 | [18] GPIO Configuration Control | 0x00 |
| [09] FPFRAME Start Position | 0x03 | [19] GPIO Status/Control | 0x00 |
| [0A] Vertical Non-Display Period | 0x0B | [1A] Scratch Pad | 0x00 |
| [0B] MOD Rate | 0x00 | [1B] Portrait Mode | 0x00 |
| [0C] Screen 1 Start Adress (LSB) | 0x00 | [1C] Line Byte Count | 0x00 |

**Note:** These values result from a Frame Rate of 65 Hz, an input clock of 12 MHz and a 8 bit-per-pixel display mode.

## 9.5 STN QVGA, 16 Greyscales, 5V, neg. $V_{EE}$ (MGLS320240, SP14 a.e.)




| Register | Value | Register | Value |
|---|---|---|---|
| [01] Mode Register 0 | 0x1C | [0D] Screen 1 Start Adress (MSB) | 0x00 |
| [02] Mode Register 1 | 0x90 | [0E] Screen 2 Start Adress (LSB) | 0x00 |
| [03] Mode Register 2 | 0x03 | [0CF] Screen 2 Start Adress (MSB) | 0x00 |
| [04] Horizontal Panel Size | 0x27 | [10] Start Adress (MSBs) | 0x00 |
| [05] Vertical Panel Size (LSB) | 0xEF | [11] Memory Adress Offset | 0x00 |
| [06] Vertical Panel Size (MSB) | 0x00 | [12] Screen 1 Vertical Size (LSB) | 0xFF |
| [07] FPLINE Start Position | 0x00 | [13] Screen 1 Vertical Size (MSB) | 0x03 |
| [08] Horizontal Non-Display Period | 0x02 | [18] GPIO Configuration Control | 0x00 |
| [09] FPFRAME Start Position | 0x03 | [19] GPIO Status/Control | 0x00 |
| [0A] Vertical Non-Display Period | 0x0B | [1A] Scratch Pad | 0x00 |
| [0B] MOD Rate | 0x00 | [1B] Portrait Mode | 0x00 |
| [0C] Screen 1 Start Adress (LSB) | 0x00 | [1C] Line Byte Count | 0x00 |

**Note:** These values result from a Frame Rate of 71 Hz, an input clock of 12 MHz and a 8 bit-per-pixel display mode.

## 10 MECHANICAL OUTLINE

PCB Frontside

