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PART NO. : **MS-10-0069**

FOR MESSRS. :

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洪 2009.05.05 登正

ACCEPTED BY: PROPOSED BY :

RECORD OF REVISION

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△1	2004/04/16	2 (△1)	P.27	Change the correct character patterns, please refer to mark △1
△2	2008/01/31	3 (△2)	P.31	Add the item 9.2 Controller ic manufacturer mark
△3	2008/02/16	4 (△3)	P.7~8	Modify the Chapter 5. Timing characteristics
			P.21~22	Modify the Chapter 6.21 Initializing by instruction
			P.29	Add the inspection item：SLANT
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	2009/05/04	5 (△4)	P.28	8.Modify the Quality and reliability: 8-4.Add the appearance test condition
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3. Precautions for LCM

3.1 Precautions in handling LCD Modules (hereinafter LCM's)

WAYTON technology's LCM's have been assembled and accurately calibrated before delivery.

Please observe the following criteria when handling.

A. Do not subject the module to excessive shock.
B. Do not modify the tab on the metal holder.
C. Do not tamper with the printed circuit board.
D. Limit soldering of the printed circuit board to I/O terminals only.
E. Do not touch the zebra strip nor modify its location.

3-2 Static electricity warning:

WAYTON's LCM uses CMOS LSI technology. Therefore, strict measures to avoid static electricity discharge are followed through all processes from manufacturing through shipping. When handling an LCM, take sufficient care to prevent static electricity discharge as you would any CMOS IC.

A. Do not take the LCM from its anti-static bag until it's to be assembled. LCM's are individually packaged in bags specially treated to resist static electricity. When storing, keep the LCM packed in the original bags, or store them in a container processed to be resistant to static electricity, or in an electric conductive container.

B. Always use a ground strap when handling a LCM.
Always use a ground strap while working with the module, from the time it is taken out of the anti-static bag until it is assembled. When it is necessary to transfer the LCM, once it has been taken out of the bag, always place it in an electric conductive container. Avoid wearing clothes made of chemical fibers, the use of cotton or conductive treated fiber clothing is recommended.

C. Use a no-leak iron for soldering the LCM.
The soldering iron to be used for soldering the I/O terminals to the LCM are to be insulated or grounded at the iron tip.

D. Always ground electrical apparatuses required for assembly.
Electrical apparatuses required to assemble the LCM into a product, i.e. electrical screw drivers, are to be first grounded to avoid transmitting spike noises from the motor.

E. Assure that the work bench is properly grounded.

F. Peel off the LCM protective film slowly.
The module is attached with a film to protect the display surface from contamination, damage, adhesion of flux, etc. Peeling off this film abruptly could cause static electricity to be generated, so peel the tape slowly.

G. Pay attention to the humidity in the work area.
50~60% RH is recommended.

3-3 Precautions for the soldering of an LCM

The following procedures should be followed when soldering the LCM:

A. Solder only to the I/O terminal.

B. Use a no leakage soldering iron and pay particular attention to the following:

(1) Conditions for soldering I/O terminals

Temperature at iron tip : 280℃ + 10℃

Soldering time : 3-4 sec/terminal

Type of solder : Eutectic solder (rosin flux filled)

Note: Avoid using flux, because it could penetrate the module and the module may get contaminated during cleaning. Peel off protective film after soldering of the I/O terminals is finished. By following this procedure, the surface contamination, caused by the dispersion of flux while soldering, can be avoided.

(2) Removing the wiring

When a lead wire, or a connector to the I/O terminal of the module is to be removed, remove it only after the solder at the connection has sufficiently melted since the I/O terminal is a through hole. If it is forcefully removed, it could cause the terminal to break or peel. The recommended procedure is to use a suction-type solder remover. Caution, do not reheat the I/O terminal more than 3 times.

3-4. Long-term storage

If the correct method of storage is not followed, deterioration of the display material (polarizer and oxidation of the I/O terminal plating may make the soldering process difficult. Please comply with the following procedure.

A. Store in the shipping container.

B. If the shipping container is not available, place in anti-static bags and seal the opening.

C. Store the modules where they are not subjected to direct sunlight or a fluorescent lamp.

D. Store in a temperature rang of 0℃~35℃ with low relative humidity.

3-5. Precautions in use of LCD modules

A. Do not give any external shock.

B. Do not wipe the surface with hard materials.

C. Do not apply excessive force on the surface.

D. Do not expose to direct sunlight or fluorescent light for a long time.

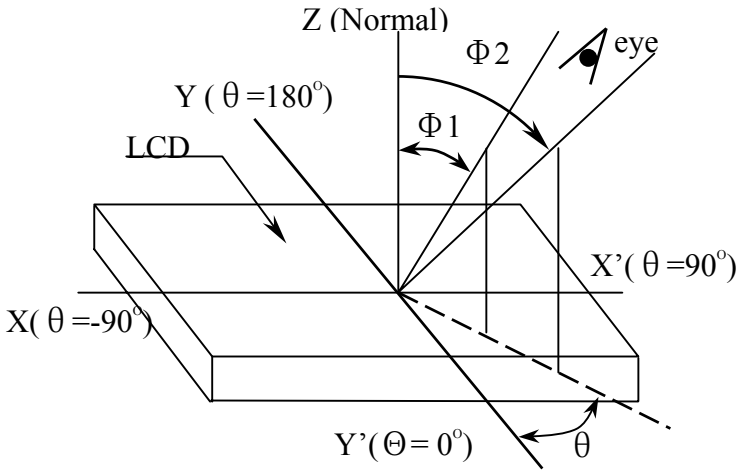
E. Avoid storage in high temperature and high humidity.

F. When storage for a long time at 40℃ or higher is required, R/H shall be less than 60%.

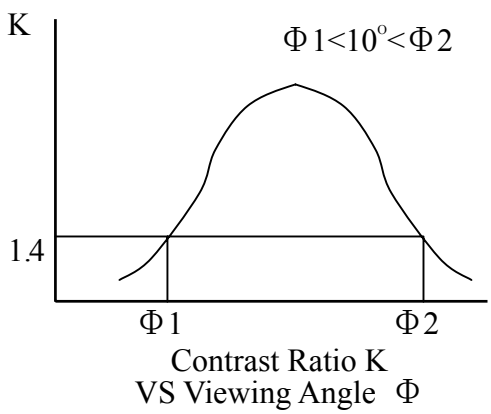
G. Liquid in LCD is hazardous substance. Must not lick, swallow when the liquid is attached to your hands, skin, clothes etc. Wash it out thoroughly.

4. Optical definitions

4.1 Definition of angle θand Φ

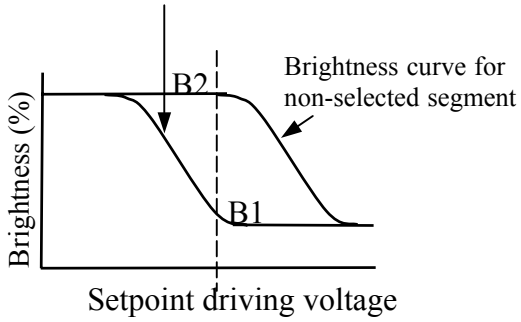


4.2 Definition of viewing angle Φ1 and Φ2

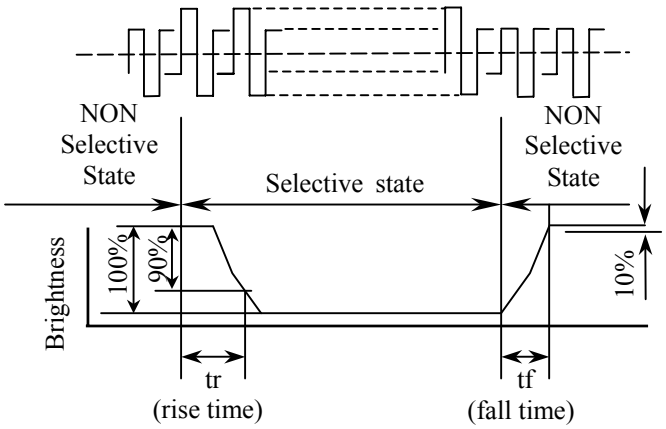


POSITIVE TYPE
4.3 Definition of contrast "K".

$$K=\frac{\text{brightness of non-selected segment (B2)}}{\text{Brightness of selected segment (B1)}}$$

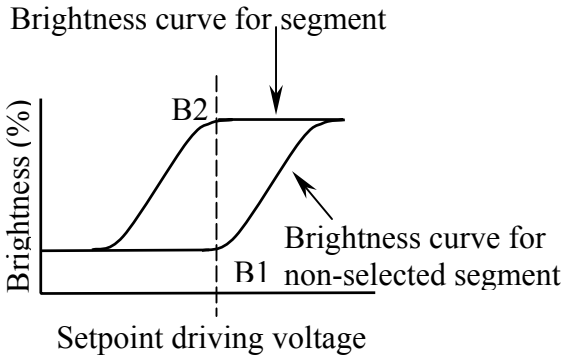


POSITIVE TYPE
4.4 Definition of optical response

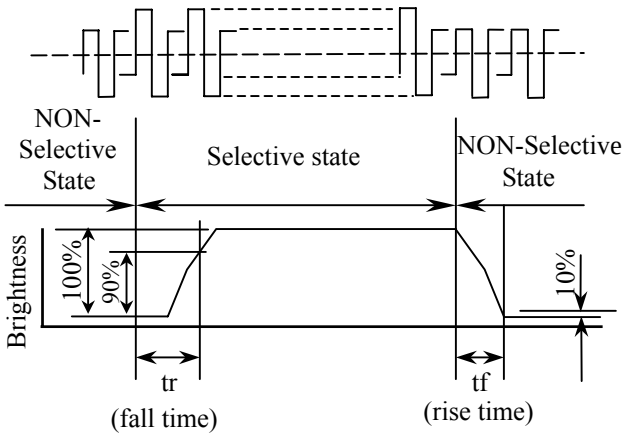


NEGATIVE TYPE
4.5 Definition of contrast "K.

$$K=\frac{\text{Brightness of selected segment (B1)}}{\text{Brightness of non-selected segment (B2)}}$$



NEGATIVE TYPE
4.6 Definition of optical response



5. Timing characteristics ⚠3

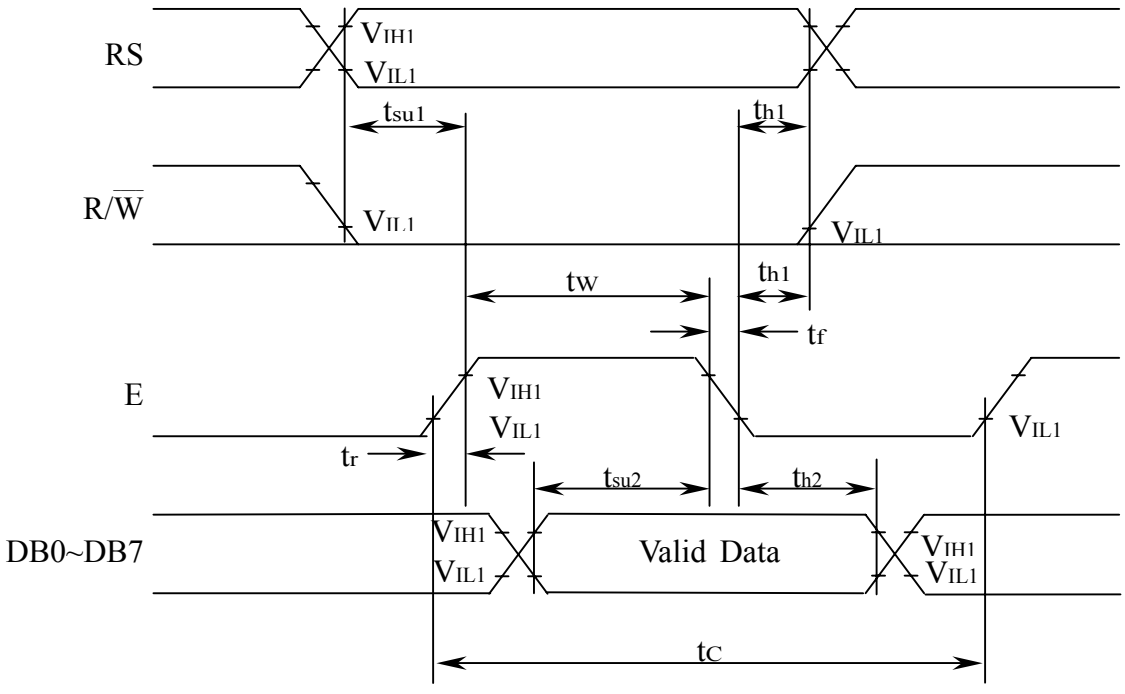
5.1 Write Operation

(a) V_{DD} = 4.5V~5.5V

Characteristics	Symbol	Min.	Typ.	Max.	Unit
E Cycle Time	tc	1200	-------	-------	ns
E Rise/Fall Time	t_R,t_F	-------	-------	25	ns
E Pulse Width	tw	230	-------	-------	ns
R/W and RS Setup Time	tsu1	40	-------	-------	ns
R/W and RS Hold Time	th1	10	-------	-------	ns
Data Setup Time	tsu2	80	-------	-------	ns
Data Hold Time	th2	10	-------	-------	ns

(b) V_{DD} = 2.7V~4.5V

Characteristics	Symbol	Min.	Typ.	Max.	Unit
E Cycle Time	tc	1200	-------	-------	ns
E Rise/Fall Time	t_R,t_F	-------	-------	25	ns
E Pulse Width	tw	460	-------	-------	ns
R/W and RS Setup Time	tsu1	60	-------	-------	ns
R/W and RS Hold Time	th1	20	-------	-------	ns
Data Setup Time	tsu2	195	-------	-------	ns
Data Hold time	th2	10	-------	-------	ns



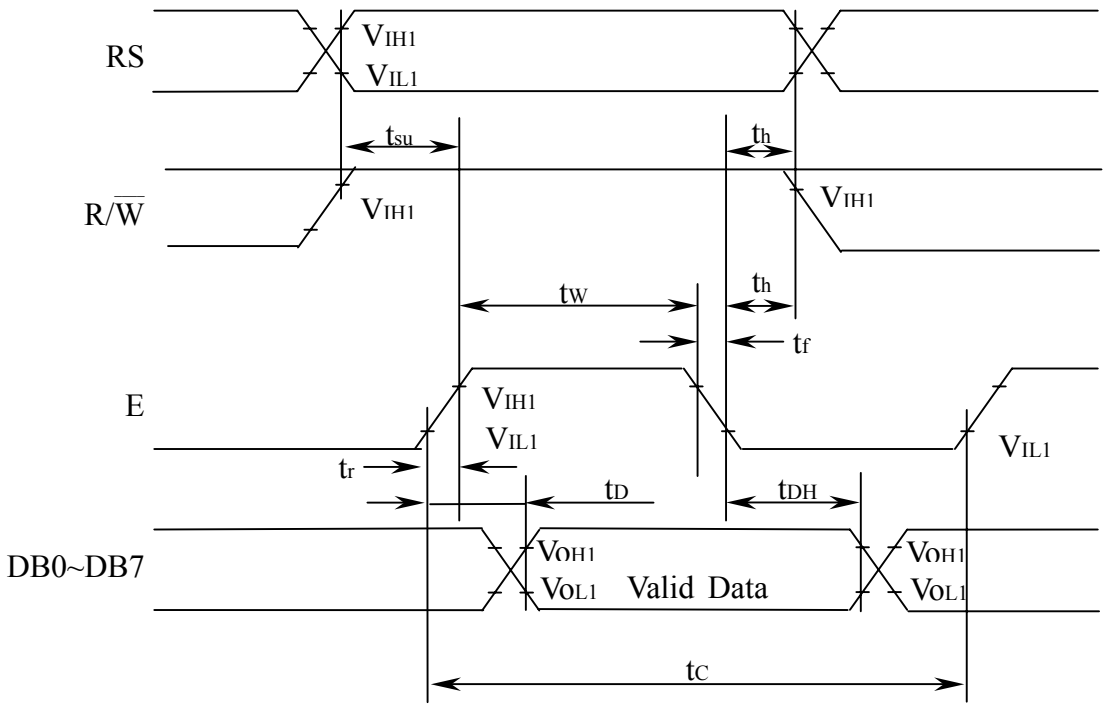
5.2 Read Operation

(a) V_{DD} = 4.5V~5.5V

Characteristics	Symbol	Min.	Typ.	Max.	Unit
E Cycle Time	tc	1200	-------	-------	ns
E Rise/Fall Time	t_R,t_F	-------	-------	25	ns
E Pulse Width	tw	230	-------	-------	ns
R/W and RS Setup Time	tsu	40	-------	-------	ns
R/W and RS Hold Time	th	10	-------	-------	ns
Data Output Delay Time	tD	-------	-------	120	ns
Data Hold time	tDH	20	-------	-------	ns

(b) V_{DD} = 2.7V~4.5V

Characteristics	Symbol	Min.	Typ.	Max.	Unit
E Cycle Time	tc	1200	-------	-------	ns
E Rise/Fall Time	t_R,t_F	-------	-------	25	ns
E Pulse Width	tw	480	-------	-------	ns
R/W and RS Setup Time	tsu	60	-------	-------	ns
R/W and RS Hold Time	th	20	-------	-------	ns
Data Output Delay Time	tD	-------	-------	360	ns
Data Hold time	tDH	10	-------	-------	ns



6 Function of each block

6.1 Register

The LSI has two 8-bit registers. One is an instruction register (IR), and the other is a data register (DR).

The IR is used to store an instruction code or an address data for a display data RAM (DD RAM) or a character generator RAM (CG RAM). The IR can be written by the MPU, but it can't be read by the MPU.

The DR temporarily stores the data to be written into the DD RAM or the CG RAM, and the data to be read out from the DD RAM or the CG RAM. In the write sequence, the data written into the DR is automatically written into the DD RAM or the CG RAM. In the read sequence, when the address data is written into the IR, the data is automatically read into the DR from the DD Ram. Then the data can be read from the DR by the MPU. After the MPU reads the DR, the address data is automatically increased or decreased for the next read from the MPU.

The relation between RS. R/$\overline{W}$ and the operation is as show below.

RS	R/$\overline{W}$	OPERATION
0	0	IR write
0	1	Read busy flag (DB7) and address counter (DB0~DB6)
1	0	DR write
1	1	DR read

6.2 Busy flag (BF)

While the instruction is executed, the busy flag is set. (Busy flag read instruction is excluded.) As a result of the status read, you can find whether the busy flag is set or not. While the busy flag is set, the LSI can't accept any other instructions than the busy flag read. Therefore, please oake sure the busy flag is reset before the issue of instruction.

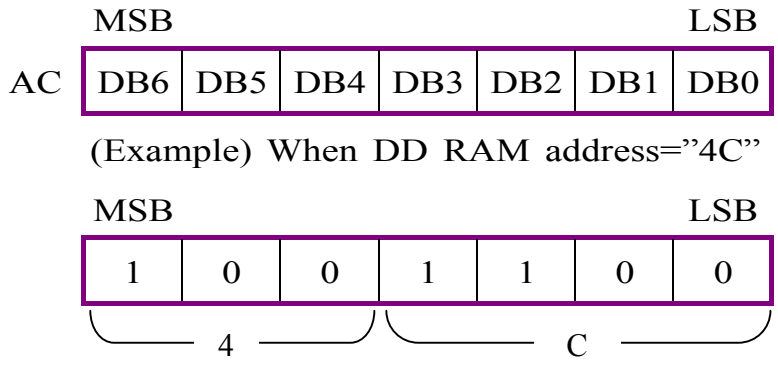
6.3 Address counter (AC)

The LSI has a 7-bit address counter. The address counter assigns the address to DD RAM, CG RAM, and the cursor control circuit. When the instruction code for DD RAM address or CG RAM address setting is written in IR, the address data is automatically sent to AC from IR. At that time, a choice between DD RAM and CG RAM is also determined by the instruction. After writing into (or reading from) DD RAM or CG RAM data. AC is automatically increased (or decreased). When RS-0, R/$\overline{W}$-1, AC data is output to DB0~DB6.

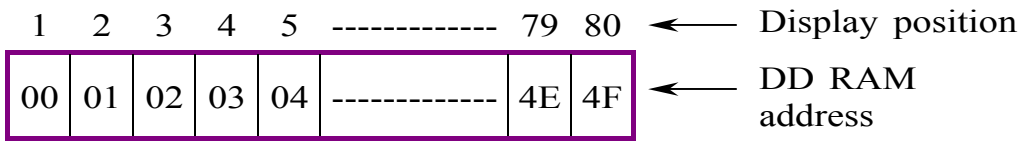
6.4 Display data RAM (DD RAM)

This Display Data RAM (DD RAM) is used to store the display data of 8-bit character codes. Its capacity is 80 characters * 8 bits. The relation between DD RAM address and Display position is as shown below.

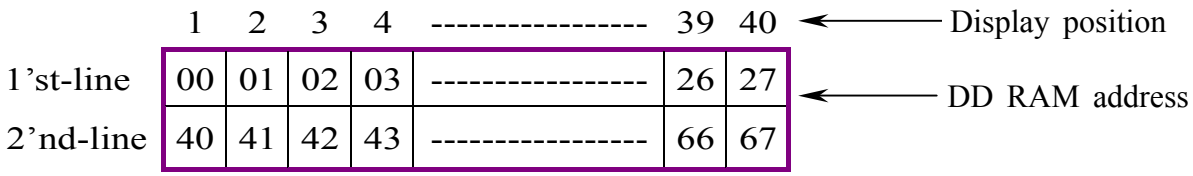
DD RAM address is expressed in hexadecimal as shown below.



(1) The relation between DD RAM address and Display position in the 1-line display mode (N=0)



(2) The relation between DD RAM address and Display position in the 2-Line display mode (N=1)



Note: The last address of the 1'st-line is not continuous to the head address of the 2'nd-line.

6.5 Character generator ROM (CG RAM)

The character generator RAM is used to display user's original character patterns. (5 * 7 dots * 8 types or 5 * 10 dots * 4 type).

The relation between character codes and CG RAM address and character patterns is shown as below.

(a) In the ease of 5 * 7 dots character patterns

Character codes (DD RAM Data)	CG RAM Address		Character Patterns (CG RAM Data)	
7 6 5 4 3 2 1 0	5 4 3 2 1 0		7 6 5 4 3 2 1 0	
0 0 0 0 * 0 0 0	0 0 0	0 0 0	* * *	0
		0 0 1		0 0 0
		0 1 0		0 0 0
		0 1 1		0
		1 0 0		0 0 0
		1 0 1		0 0 0
		1 1 0		0
		1 1 1	* * *	0 0 0 0 0 ← Position
0 0 0 0 * 0 0 1	0 0 1	0 0 0	* * *	0
		0 0 1		0 0 0 0
		0 1 0		0 0 0 0
		0 1 1		0 0
		1 0 0		0 0 0 0
		1 0 1		0 0 0 0
		1 1 0		0
		1 1 1	* * *	0 0 0 0 0 ← Position
		0 0 0	* * *	
		0 0 1		0 0 0 0
0 0 0 0 * 1 1 1	1 1 1	0 1 1	* * *	0 0 0 0
		1 0 0		0 0 0 0
		1 0 1		0 0 0 0
		1 1 0		0 0 0 0
		1 1 1	* * *	0 0 0 0 0 ∴:Invalid

Character Pattern Example (1) Cursor

Character Pattern Example (2) Cursor

Note 1.: Character code bits 0~2 correspond to CG RAM address bits 3~5.

2.: CG RAM address bits 0~2 designate character pattern line position. The 8'th line is in the cursor position and it is displayed in logical or by the cursor. Therefore the 8'th line data correspond to the cursor display position must be "0" state for cursor display. When the 8th line data is "1", the bit lights up regardless of cursor existence.

3.: Character pattern line positions correspond to CG RAM data bits 0~4. As CG RAM data bits 5~7 are not used for display, they can be used for the general data RAM.

4.: When character code bits 4~7 are all "0", CG RAM character patterns are selected. As character code bit 3 is an invalid bit, character code 1100 and 0811 selects the same character pattern.

5.: "1": ON Data "0": OFF Data

(a) In the case of 5 * 10 dots character patterns

Character codes (DD RAM Data)	CG RAM Address	Character Patterns (CG RAM Data)
7 6 5 4 3 2 1 0	5 4 3 2 1 0	7 6 5 4 3 2 1 0
0 0 0 0 * 0 0 *	0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 1 1 0 0 1 0 0 0 0 0 1 0 1 0 0 1 1 0 0 0 1 1 1 0 1 0 0 0 0 1 0 0 1 0 1 0 1 0	* * * * * * 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1 1 0 0 0 0 0 0
⋮	⋮ 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	* *
0 0 0 0 * 1 1 *	1 1 0 0 0 0 0 0 0 1 0 0 1 0 1 0 0 0 1 0 0 1 1 0 1 0	* * * * * *
⋮	⋮ 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	* *

Character Pattern Example (1)

Cursor ← Position

∴:Invalid

Note 1.: Character code bits 1, 2 correspond to CG RAM address bits 4, 5.

2.: CG RAM address bits 0~3 designate character pattern line position. The 11'th line is in the cursor position and it is displayed in logical or by the cursor. Therefore the 11'th line data correspond to the cursor display position must be "0" state for cursor display. When the 11'th line data is "1", the bit lights up regardless of cursor existence. As the 12'th~16'th lines aren't used for display, they can be used for the general data RAM.

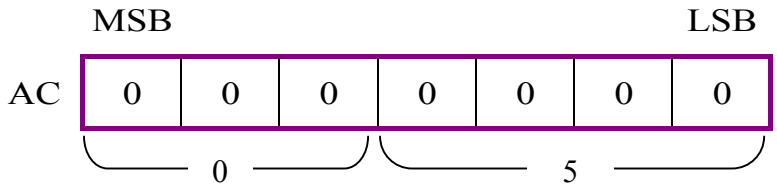
3.: When character code bits 4~7 are all "0", CG RAM character patterns are selected. As character code bit 0 and 3 are invalid bit, character code 0011, 0111, 0811 and 0911 select the same character pattern.

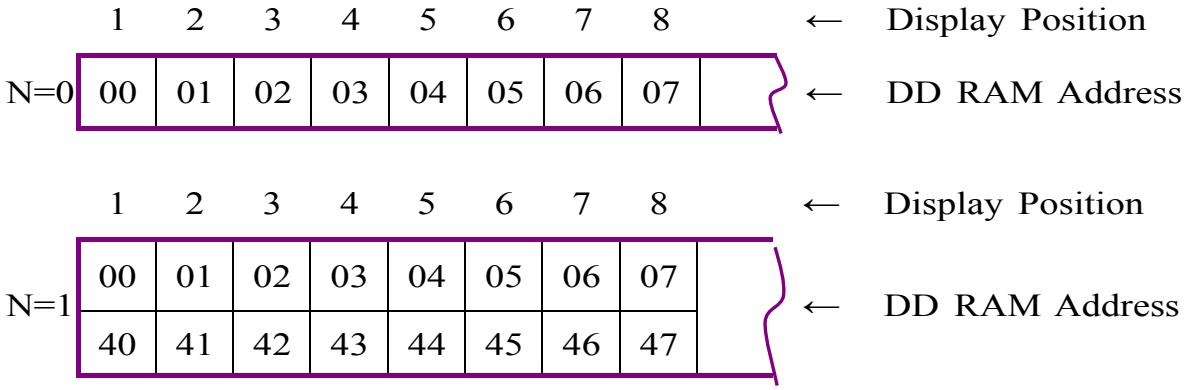
4.: "1": ON Data "0": OFF Data

6.6 Cursor/blink control circuit

This circuit generates the cursor or blink. The cursor or blink appears in the digit corresponding to the display data RAM (DD RAM) address set in the address counter (AC).

When the address counter is 0511, the cursor appears as shown below





Note: The cursor or blink also appears when the character generator RAM (CG RAM) address is set in the address counter (AC).
Therefore the cursor or blink appears regardless of the display data RAM (DD RAM) address.

6.7 Internal reset circuit

When the power is turned on, the LSI is automatically initialized using the internal reset circuit. The busy flag (BF) is held "1" (busy state) until the initialization ends. The following instruction are executed in initialization.

(1) Display Clear

(2) Function Set ..... DL = 1: 8-bit data interface
N = 0: 1-line display
F = 0: 5 * 7 dots character font

(3) Entry mode set ..... I/D = 1: +1
S = 0: No shift

(4) Display ON/OFF control ..... D = 0: Display OFF
C = 0: Cursor OFF
B = 0: Blink OFF

6.8 Interfacing to MPU

The LSI has two method of interfacing to MPU. One is 8-bit data interface and the other is 4-bit data interface.

(1) When the interface data length is 4-bit the data is transferred using 4 data buses (DB4~DB7). The other data buses (DB0~DB3) are not used. The data is transferred from the MPU to the LSI in twice. After the higher order 4-bit data (contents of DB4~DB7) when the interface data is 8-bit length is transferred first, the lower order 4-bit data (contents of DB0~DB3 when the interface data is 8-bit length) is transferred. The busy flag and address counter data is also transferred in twice.

(2) When the interface data length is 8-bit the data is transferred using 8-data buses (DB0~DB7).

6.9 Instruction

The MPU can directly control only two registers. One is instruction Register (IR) and the other is Data Register (DR).

When an instruction is executing, no instruction other than the busy flag/address read instruction will be executed. As the busy flag is held "1" (busy state until an instruction ends, before sending the instruction from the MPU to the LSI, the MPU must check that the busy flag is "0" (not busy state).

If the instruction is sent without checking the busy flag, the instruction is sent without checking the busy flag, the instruction cycle is much longer than the instruction time.

Instruction	CODE										Description	Execution Line (MAX.) (fcp=250KHz)
	RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0		
Test	0	0	0	0	0	0	0	0	0	0	Don't use.	0μs
Clear display	0	0	0	0	0	0	0	0	0	1	Clear all display and sets DD RAM address 0 in address counter	1.53 ms
Return home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter and return display to home position. The contents of DD RAM don't change.	1.53 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operation are executed, when data read and write.	39μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	39μs
Cursor / display shift	0	0	0	0	0	1	S/C	R/L	*	*	Shifts cursor and display without changing DD RAM contents.	39μs
Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N), and character font (F).	39μs
Set CG RAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Sets CG RAM Address.	39μs
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Sets DD RAM Address.	39μs
Read busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Reads busy flag (BF), and address counter contents.	0μs
Write data To CG OR DD RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into DD RAM or CG RAM.	43μs
Read data From CG or DD RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Reads data into DD RAM or CG RAM.	43μs
	I/D = 1: Increment S = 1: Accompanies display shift S/C = 1: Display shift R/L = 1: Shift to the right DL = 1: 8 bits N = 1: 2 lines F = 1: 5 * 10 dots BF = 1: Internally operating BF = 0: Can accept instruction							I/D = 0: Decrement S/C = 0: Cursor move R/L = 0: Shift to the left DL = 0: 4 bits N = 0: 1 line F = 0: 5 * 7 dots					-------

6.10 Clear display

	RS	R/$\overline{W}$	DB7							DB0
Instruction Code	0	0	0	0	0	0	0	0	0	1

When this instruction is executed, the space code “20” (Character code “20” must be blank pattern) is written into all DD RAM address in the address counter is reset.

In other words, the display disappears and the cursor or blink goes to the left end (of the first line in the 2-line display mode) I/D of Entry mode is set (increment mode).

S of Entry mode doesn’t change.

6.11 Return home

	RS	R/$\overline{W}$	DB7							DB0
Instruction Code	0	0	0	0	0	0	0	0	1	*

*: Invalid

When this instruction is executed, DD RAM address in the address counter is reset. When the display is shifted, it returns to its home position. The contents of DD RAM don’t change. The cursor or blink goes to the left end of the display (The left end of the first line in the 2-line display mode).

6.12 Entry mode set

	RS	R/$\overline{W}$	DB7							DB0
Instruction Code	0	0	0	0	0	0	0	1	I/D	S

I/D: When a character code is written into or read from the DD RAM the DD RAM address is increased (I/D=1) or decreased (I/D=0) by 1.

When I/D=1, the cursor or blink moves to the right. When I/D=0 the cursor or blink coves to the left. The same applies to writing or reading of CG RAM.

S When S=1 and I/D=1, the entire display shifts to the left at the time for writing to the DD RAM.

When S=1 and I/D=0, the entire display shifts to the rights.

Therefore, the cursor position looks as if it stands still and the display moves.

The display doesn’t shift at the time of reading from the CG RAM.

When S=0, the display doesn’t shift.

6.13 Display ON/OFF control

	RS	R/$\overline{W}$	DB7						DB0
Instruction Code	0	0	0	0	0	0	1	D	C	B

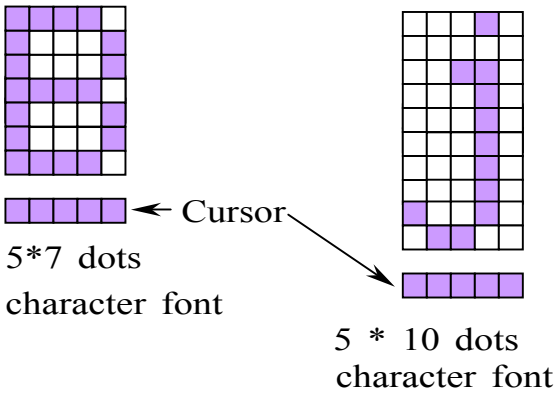
D: When D=1, the display is ON. When D=0, the display is OFF.
When D is reset, DD RAM contents don't change. Therefore, it can be displayed as before by setting D.

C: When c=1, the cursor display. When C=0, the cursor doesn't display
When the 5*7 dots character font is selected, the cursor is display using 5 dots in the 8'th line.
When the 5*10 dots character font is selected, the cursor is displayed using 5 dots in the 11'th line.

B: When B=1 the character corresponding to the cursor position blinks.
The blink is displayed by switching between all ON dots and display characters at 409.6ms (5 * 7 dots character font) or 563.2ms (5 * 10 dots character font) internal when fosc-250KHz. The cursor and the blink can be set to display simultaneously.

˙5 * 7 dots character font (fcp = 250 KHz)

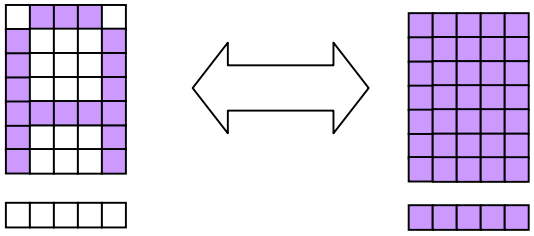
$\frac{1}{250k}$ *5 * 80 * 8 * 32 = 409.6 (mesc)



(a) Cursor Display Example

˙5 * 10 dots character font (fcp = 250 KHz)

$\frac{1}{250k}$ *5 * 80 * 11 * 32 = 563.2 (mesc)



(b) Blink Display Exampl

6.14 Cursor or display shift

	RS	R/$\overline{W}$	DB7							DB0	
Instruction Code	0	0	0	0	0	1	S/C	R/L	*	*	*: Invalid

When this instruction is executed, the cursor or display is shifted to the right or left without writing or reading display data.

In the 2-line display mode, the cursor is shifted from the 40'th digit of the 2'nd line displays shift at the same time, and only shift horizontally.

S/C	R/C	FUNCTIONS
0	0	Shift the cursor to the left
0	1	Shift the cursor to the right
1	0	Shift the all display to the left. The cursor follows the display shift.
1	1	Shift the all display to the right. The cursor follows the display shift.

When S/C=1, Address Counter (AC) contents don't change.

6.15 Function set

	RS	R/$\overline{W}$	DB7	----------					DB0
Instruction Code	0	0	0	0	1	DL	N	F	*	*

DL: When DL=1, Data is transferred in 8-bit length. (DB0~DB7).
When DL=0, Data is transferred in 4-bit length. (DB4~DB7).

N: When N=0, 1-line display mode is selected.
When N=1, 2-line display mode is selected.

F: When F=0, 5*7 dots character font is selected.
When F=1, 5*10 dots character font is selected.

Note: Execute this instruction at the head of the program before executing all instructions. (except busy flag/address read).
After that time, this instruction can't be executed unless the interface data length is changed.

N	F	No. Of display lines	Character font	Duty	NOTE
0	0	1	5 * 7 dots	1/8	----------
0	1	1	5 * 10 dots	1/11	----------
1	*	2	5 * 7 dots	1/16	When N=1, 5*10 dots character font can't be selected.

6.16 Set CG RAM address

	RS	R/$\overline{W}$	DB7							DB0
Instruction Code	0	0	0	1	A	A	A	A	A	A
					MSB					LSB

When this instruction is executed, the CG RAM address is set into the address counter in binary AAAAAA. Since then, the MPU reads or writes the data for the CG RAM.

6.17 Set DD RAM address

	RS	R/$\overline{W}$	DB7							DB0
Instruction Code	0	0	1	A	A	A	A	A	A	A
				MSB						LSB

When this instruction is executed, the DD RAM address is set into the address counter in binary AAAAAAA. Since then, the MPU reads or writes the data for the DD RAM.

6.18 Read busy flag and address

	RS	R/$\overline{W}$	DB7							DB0
Instruction Code	0	1	BF	A	A	A	A	A	A	A
				MSB						LSB

When this instruction is executed, the busy flag and the address counter contents are output. The busy flag indicates whether the instruction can be received or not. The MPU must check that the busy flag is “0” (not busy state), before sending the instruction to the LSI

The address counter indicate the CG or DD RAM address.

The previous instruction (Set CG RAM Address or Set DD RAM Address) determines whether the Address counter indicate the CG RAM or DD RAM Address.

6.19 Write data to CG or DD RAM

	RS	R/$\overline{W}$	DB7							DB0
Instruction Code	1	0	D	D	D	D	D	D	D	D
			MSB							LSB

When this instruction is executed, the binary 8-bit data DDDDDDDD is written to the CG or DD RAM. The previous instruction (Set CG RAM Address or Set DD RAM Address) determines whether the data is written to the CG RAM or DD RAM. After writing the address is automatically increased or decreased by 1 according to the entry mode. The display mode is also determined by the entry mode.

6.20 Read data from CG or DD RAM

	RS	R/$\overline{W}$	DB7							DB0
Instruction Code	1	1	D	D	D	D	D	D	D	D
			MSB							LSB

When this instruction is executed, the binary 8-bit data DDDDDDDD is read from the CG or DD RAM. The previous instruction (Set CG RAM Address) determines whether the data is read from the CG RAM or DD RAM. Before executing this instruction, the CG RAM or DD RAM address set instruction must be executed. If you don't, the first read data will be invalidated. When continuously executing the read instruction, the next address data is normally read from the second read. But, when the cursor is shifted by the cursor shift instruction, the address set instruction need not be executed just before the read instruction (when reading DD RAM). The operation of the cursor shift instruction is the same as that of the DD RAM address set instruction.

After reading, the address is automatically increased by 1. And it is determined by the entry mode. But, the display Shift is not executed regardless of the entry mode.

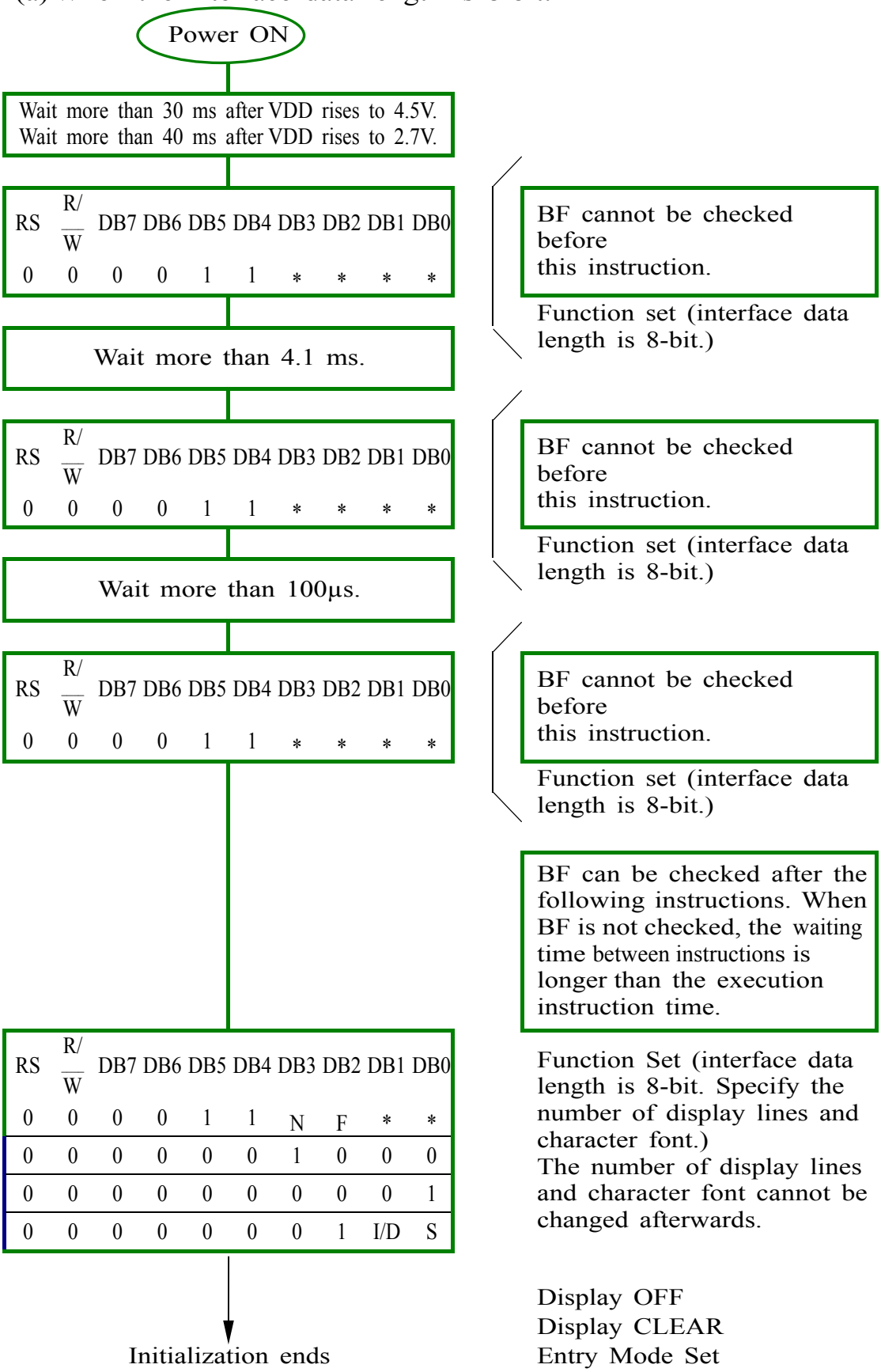
NOTE: After the write instruction to CG RAM or DD RAM, the address counter (AC) is automatically increased or decreased by 1. But, the RAM data selected by the AC counter can't be read out even though the read instruction is immediately executed. The conditions of the correct data are executing of the address set instruction or cursor shift instruction (only with DD RAM) just before the reading instruction , executing of the read instruction after the 2'nd read instruction.

6.21 Initializing by instruction

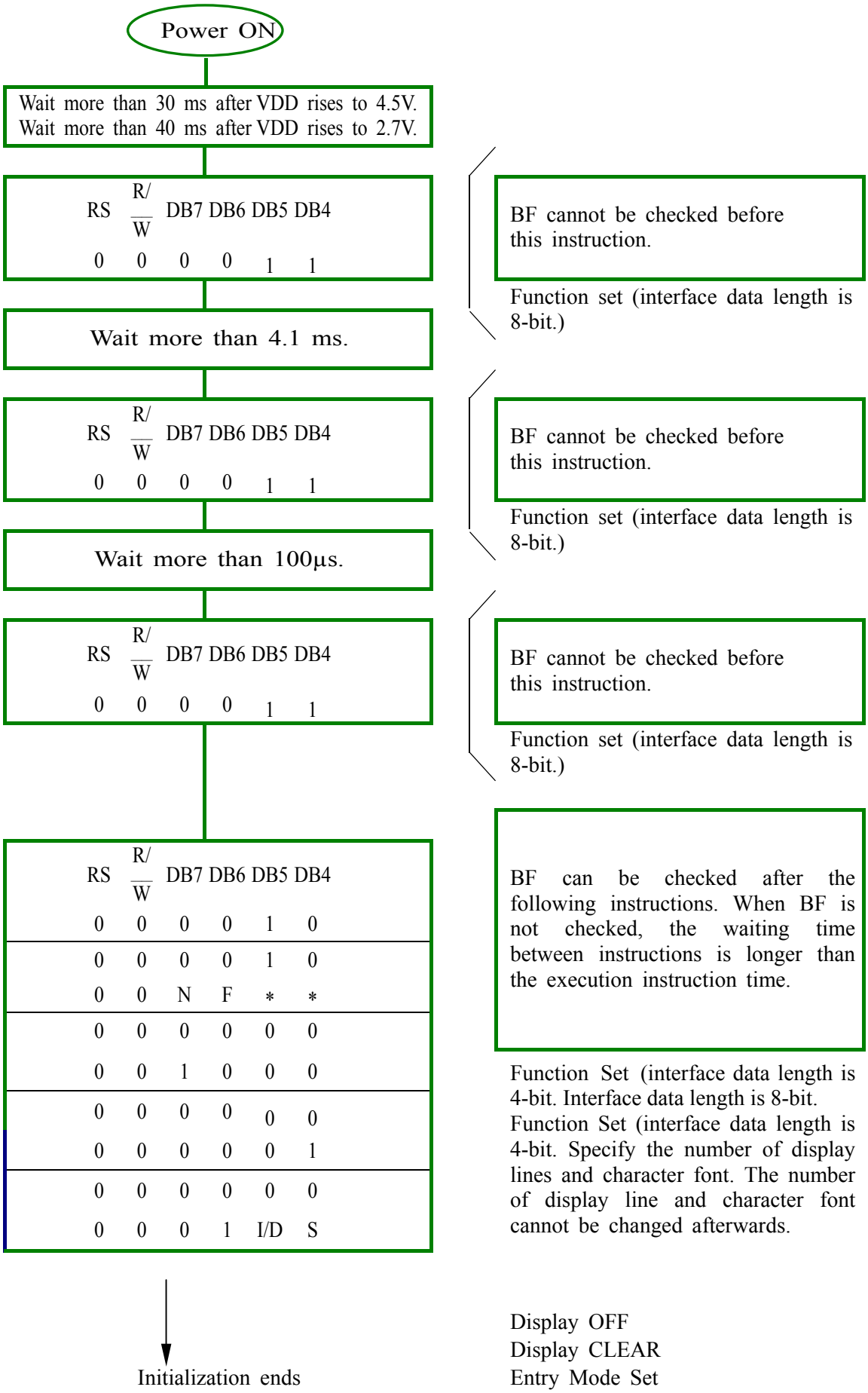
△3 If the internal reset circuit doesn't operate correctly, initialization by instruction is required.

Use the following procedure for initialization.

(a) When the interface data length is 8-bit:



(b) When the interface data length is 4-bit



7. Character generator ROM(CG ROM)

(a) Character Fonts

Nil:S6A0069-0

The relationship between character codes and Character Patterns

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															

(b)Character Fonts(for B)

B:SED1278-D0B

The relationship between character codes and Character Patterns

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)															
		0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*A*	*B*	*C*	*D*	*E*	*F*
	0	CG RAM (1)															
	1	CG RAM (2)															
	2	CG RAM (3)															
	3	CG RAM (4)															
	4	CG RAM (5)															
	5	CG RAM (6)															
	6	CG RAM (7)															
	7	CG RAM (8)															
	8	CG RAM (1)															
	9	CG RAM (2)															
	A	CG RAM (3)															
	B	CG RAM (4)															
	C	CG RAM (5)															
	D	CG RAM (6)															
	E	CG RAM (7)															
	F	CG RAM (8)															

(c)Character Fonts(for K)

K: S6A0069-08

The relationship between character codes and Character Patterns

Upper 4bit / Lower 4bit	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)														
LLLH	CG RAM (2)														
LLHL	CG RAM (3)														
LLHH	CG RAM (4)														
LHLL	CG RAM (5)														
LHLH	CG RAM (6)														
LHHL	CG RAM (7)														
LHHH	CG RAM (8)														
HLLL	CG RAM (1)														
HLLH	CG RAM (2)														
HLHL	CG RAM (3)														
HLHH	CG RAM (4)														
HHLL	CG RAM (5)														
HHLH	CG RAM (6)														
HHHL	CG RAM (7)														
HHHH	CG RAM (8)														

(d) Character Fonts(for L)

L: S6A0069-19

The relationship between character codes and Character Patterns

Upper 4bit / Lower 4bit	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)														
LLLH	CG RAM (2)														
LLHL	CG RAM (3)														
LLHH	CG RAM (4)														
LHLL	CG RAM (5)														
LHLH	CG RAM (6)														
LHHL	CG RAM (7)														
LHHH	CG RAM (8)														
HLLL	CG RAM (1)														
HLLH	CG RAM (2)														
HLHL	CG RAM (3)														
HLHH	CG RAM (4)														
HHLL	CG RAM (5)														
HHLH	CG RAM (6)														
HHHL	CG RAM (7)														
HHHH	CG RAM (8)														

(e) Character Fonts(for H)

⚠1 H: SED1278-D0H

The relationship between character codes and Character Patter

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															

8. Quality and reliability

8.1 Test condition

Test should be conducted under the following conditions:

Ambient temperature: 25±5℃

Humidity : 60±20% RH

8.2 Sampling plan

Sampling method shall be in accordance with MIL-STD-105D, inspection level II, normal inspection, and single sampling plan tables for normal tightened, and reduced inspection.

8.3 Acceptable quality level

A major defect is a defect that could result in failure or materially reduce that the usability of the unit of product for its intended purpose.

A minor defect is one that does not materially reduce the usability of the unit of product for its intended purpose or is a departure from established standards having no significant bearing on the effective use or operation of the unit.

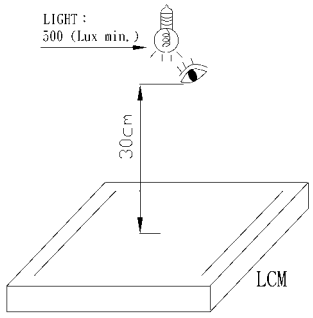
8.4 Appearance

Appearance test is to be conducted by human eyes at approximately 30cm distance from LCD module under the single fluorescent light.

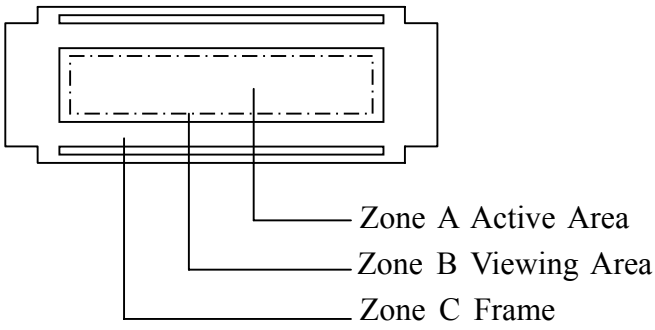
④ Condition: a. Illumination: 500 Lux min

b. Inspect determination: 30 cm

c. Inspect direction: above the LCM



The inspection area of LCD panel shall be within the range of following limits.

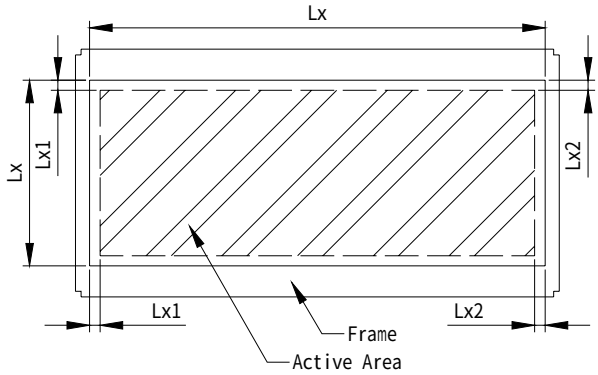


8.5 Inspection quality criteria

ITEM	DESCRIPTION OF DEFECTS	Class of defects	Acceptable level (%)
FUNCTION	Short circuit or Pattern cut	Major	0.65
DIMENSION	Refer to individual acceptance specification	Major	2.5

③ SLANT — Minor — 2.5

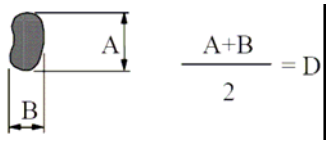
Viewing Area	| Lx1-Lx2 |	Judgment
Lx≤ 100	≤ 0.2	ACC
100 < Lx ≤ 150	≤ 0.3	ACC
150 < Lx ≤ 200	≤ 0.4	ACC
200 < Lx	≤ 0.5	ACC



③ BLACK SPOTS — Minor — 2.5

Ave. dia. D	area A	area B
D ≤0.2	disregard	
0.2 < D ≤ 0.3	2	3
0.3 < D ≤ 0.4	0	1
0.4 < D	0	0

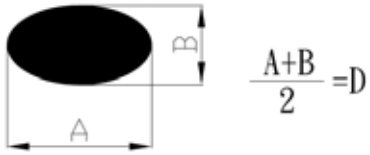
④



④ CONTRAST MURA — Minor — 2.5

Ave. dia. D	area A	area B
D ≤0.5	disregard	
0.5 < D ≤ 0.7	3	disregard
0.7 < D	0	disregard

NOTE: For LCD best driving voltage.



BLACK LINES — Minor — 2.5

Width W, Length L	A	B
W ≤ 0.03	disregard	
0.03 ′ W ≤ 0.05	3	4
0.05 ′ W ≤ 0.07, L ≤3.0	1	1

ITEM	DESCRIPTION OF DEFECTS	Class of defects	Acceptable level (%)
BUBBLES IN POLARIZER	Average diameter D 0.2 < D < 0.5 mm for N = 4 0.5 < D < 0.7 for N=1	Minor	2.5
COLOR UNIFORMITY	Rainbow color or Newton ring.	Minor	2.5
GLASS SCRATCHES	Obvious visible damage.	Minor	2.5
VIEWING ANGLE	Refer to individual acceptance specification	Minor	2.5
CONTRAST RATIO	Refer to individual acceptance specification	Minor	2.5
RESPONSE TIME	Refer to individual acceptance specification	Minor	2.5

8.6 Reliability

The LCD module should have no failure in the following reliability test.

TEST ITEM	TEST CONDITIONS	NOTE
HIGH TEMPERATURE STORAGE	70℃ , 200 hr.	NOTE
LOW TEMPERATURE STORAGE	-20℃ , 200 hr.	NOTE
HUMIDITY STORAGE	50℃ , 90%RH , 96hr.	NOTE
HIGH TEMPERATURE OPERATION	50℃, typical operating conditions, 200hr.	NOTE
LOW TEMPERATURE OPERATION	0℃, typical operating conditions, 200hr.	NOTE
TEMPERATURE CYCLING	-10℃~70℃ 10min. between each step temp. 50min. at each step temp. 5 cycles.	NOTE
MECHANICAL VIBRATION	10~100Hz sweep, 4G. amp1 =10mm(max) XYZ for 60min. each.	NOTE
MECHANICAL SHOCK	10~55Hz , 50G. XYZ for 1 time.each.	NOTE

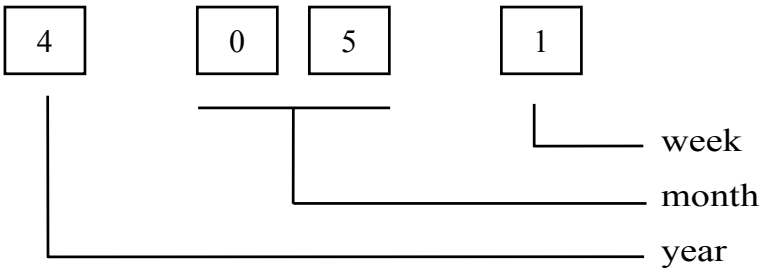
NOTE1: The module should not have condensation of water on the module.

NOTE2: The module shelled be inspected after 1 hour storage in normal conditions (15~35℃, 45~65%RH).

9. Designation of lot mark

9.1 Lot mark

Lot mark is consisted of 4 digit number.



YEAR	FIGURE IN LOT MARK
1997	7
1998	8
1999	9
2000	0
2001	1
2002	2

MONTH	FIGURE IN LOT MARK	MONTH	FIGURE IN LOT MARK
Jan.	01	July	07
Feb.	02	Aug.	08
Mar.	03	Sept.	09
Apr.	04	Oct.	10
May.	05	Nov.	11
June	06	Dec.	12

WEEK (DAY IN CALENDAR)	FIGURE IN LOT MARK
1~7	1
8~14	2
15~21	3
22~28	4
29~31	5

㉡ 9.2 Controller IC manufacturer mark

The manufacturer mark is consisted of 1 character

＊ E

MARK	MANUFACTURER
E	NEOTEC
S	SUNPLUS
W	SAMSUNG
T	SITRONIX